**2) Controller Design**

In this part, we designed a buck converter with input voltage of 24 V, output voltage of 12 V and power rating of 80 W, therefore same specifications is provided with the chosen Hardware Project. It is considered to have such numerical values for passive elements;

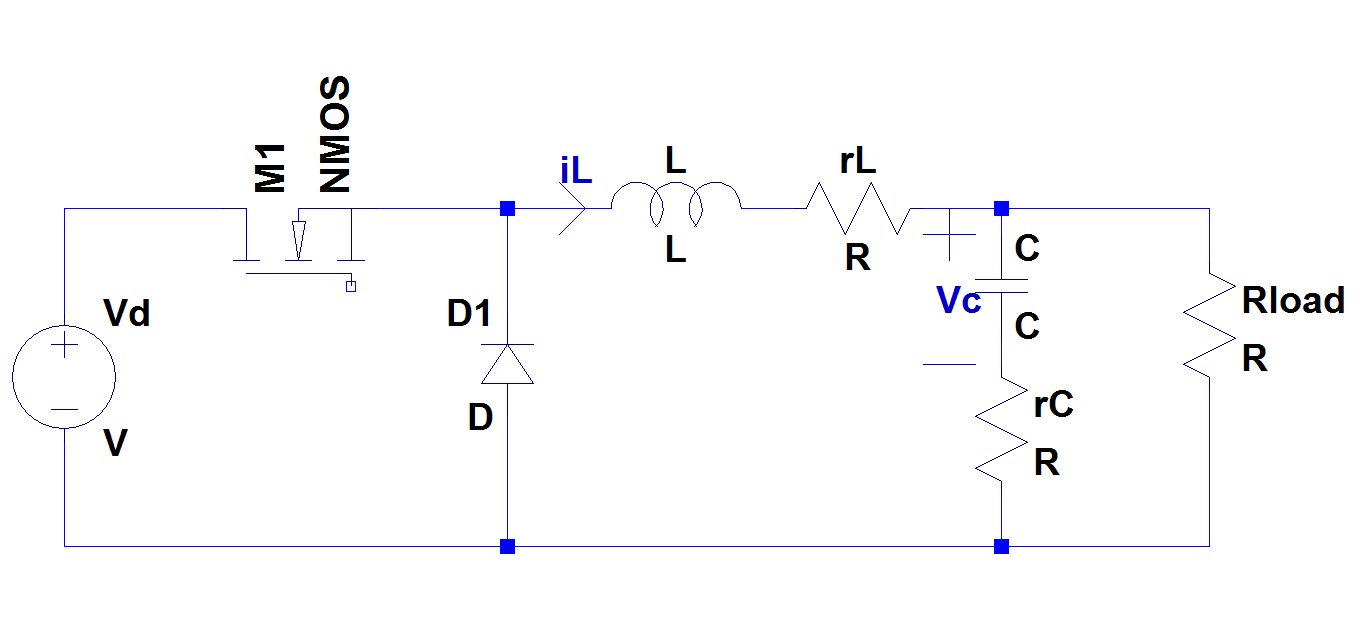
Inductance: 1 mH and Equivalent Series Resistance (ESR): 10 mΩ

Capacitance: 470µ F and Equivalent Series Resistance (ESR): 10 mΩ

**a)**

In this part, a buck converter transfer function is obtained analytically. In order to make the model realistic ESR values of both inductor and capacitor is added to converter schematic as seen in Figure 2.1. As marked in the schematic, there are two state variables in the buck converter namely inductor and capacitor current.

and Vo = C\*X where So, aim is finding A, B,C vectors.

Figure 2.1: Realistic buck converter

*On State of buck converter*

As known, LCR circuit is connected to Vd through MOSFET in on state. Hence two mesh equations can be written such that one of them is covering outer mesh which consists of input voltage, inductor and load resistor and other one is covering capacitor and load resistor.

Kirchoff Voltage Law on outer mesh:

(1)

Kirchoff Voltage Law on small mesh:

(2)

From 2nd equation;

(3)

From 1st and 3rd equation;

(4)

Hence A1 and B1 matrices can be constructed as follows

Output voltage equation;

So;

*Off State of buck converter*

At off state, LCR circuit is short circuited through diode. Note that off state is exactly same with on state with Vd short circuited. So A2 = A1 and B2 = 0. Also output voltage equation is same which yields C2 = C1.

Resultant matrices;

A = A1 = A2 B= B1\*D C= C1= C2

As ESR of the inductor and capacitor is usually in mΩ range and minimum Rload is about 1.8Ω a reasonable assumption can be done with Rload >>rC,rL also Rload>>rC+rL. Resultant matrices can be constructed as follows;

*Obtaining Transfer Function*

From Mohan’s book at page 325 this transfer function formula can be seen;

C:\Users\St\Desktop\mohan tf.png

By substituting matrices found before it can be expressed as follows;

Taking inverse of middle matrices;

Hence;

Substituting numerical values; C =470 µF, L =1 mH, rC =10 mΩ, rL = 10 mΩ and R =1.8 Ω

Note that the terms results from rC and rL makes very small effect in denominator, but rC results a zero which may causes considerable differences at high frequencies. Bode plot of this transfer function is obtained using MATLAB, related result can be seen in Figure 2.2. Some comments can be done here as follows. Transfer function has fixed gain and small phase at low frequencies. Magnitude makes a fall with -40 dB/decade beyond the cut off frequency which is located at √(1/LC) and phase approaching -180°. Then slope decreased to -20 dB/decade where zero introduced by capacitor ESR and phase goes to -90°.

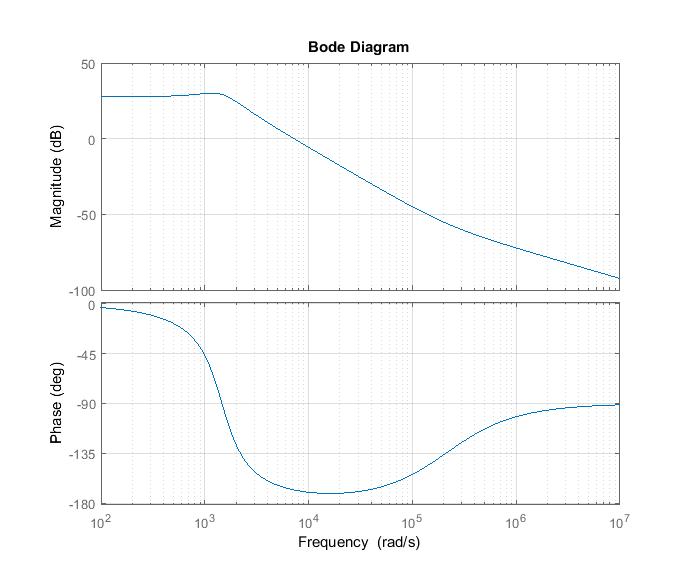


Figure 2.2: Bode plot of analytically calculated transfer function

**b)**

In this part, transfer function of the buck converter is simulated in order to obtain same transfer function with previous part. PSIM is chosen as simulation environment. The schematic which can be seen in Figure 2.3 is constructed by following procedure explained by official PSIM account on [YouTube](https://www.youtube.com/watch?v=nbFo-NMeY_w). As a result, bode plot which can be seen in Figure 2.4 is obtained.

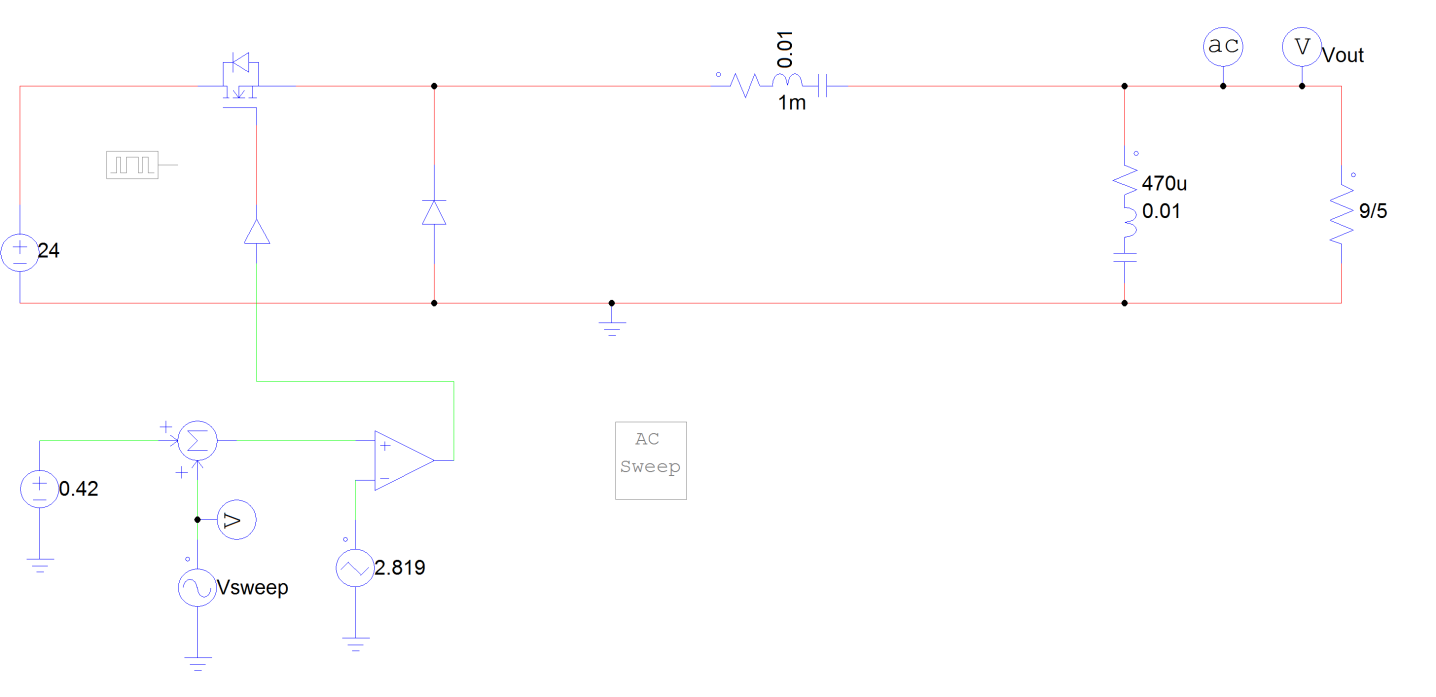


Figure 2.3: The schematic circuit of the designed Buck Converter

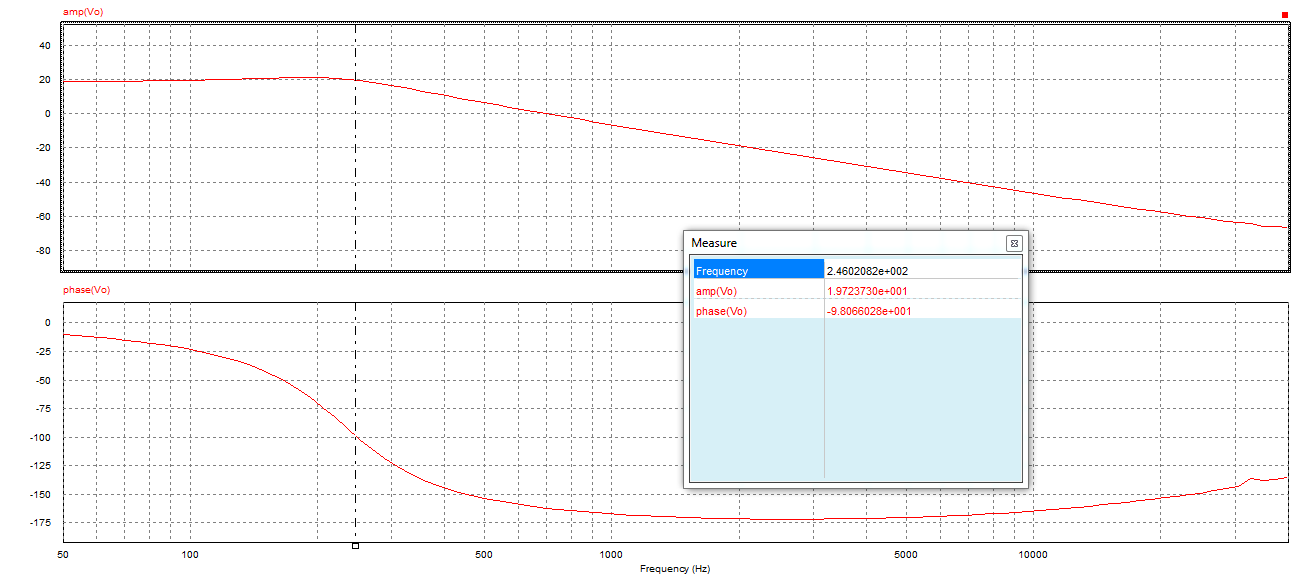


Figure 2.4: The Bode plot of the simulated Buck Converter

As can be seen in both bode plot graphs namely Figure 2.2 and Figure 2.4, they are same noting that one of them is plotted to rad/s while other is plotted to Hz. As a consequence, it can be noted here that phase margin of the converter is about 20° and it should be improved by adding phase at the gain cross over frequency with the Type-2 controller in order to have more stable converter and better transient performance.

**c)**

In this part, Type-2 controller will be constructed in order to increase phase margin of the converter. Therefore, transient stability can be provided.

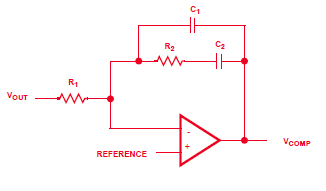


Figure 2.5: Type-2 compensator

Transfer function of the compensator is

This transfer function has one zero at 1/ and two pole at 0 and1/ . In order to increase the phase margin of the converter bode plot which is in Figure 2.2, zero of the compensator should located around 103 rad/s and nonzero pole should be located around 105-106 rad/s. Let choose R2 = 1kΩ so C2 = 1µF and C1 =1nF. Note that R1 is just adjusting gain. As R1 should be very large in order to have very low gain where gain is constant, let R1 = 100MΩ. The resultant bode plot can be seen in Figure 2.6.

From this point on, simulations are conducted on SIMULINK.

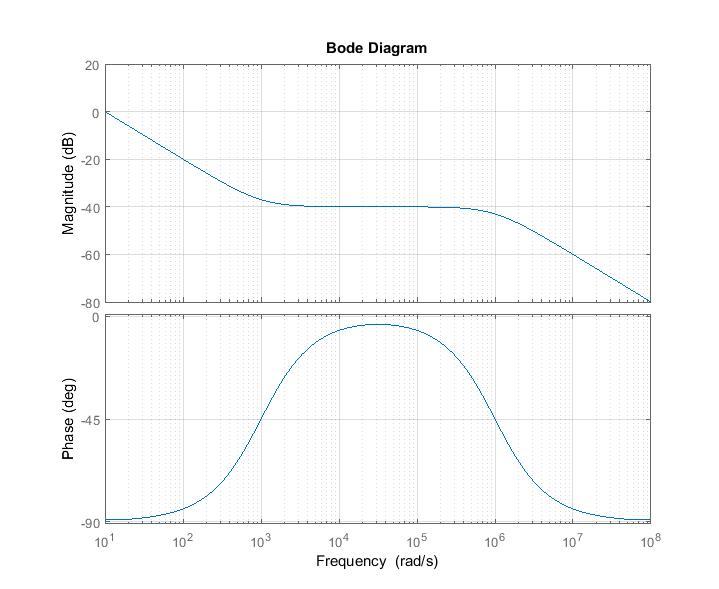
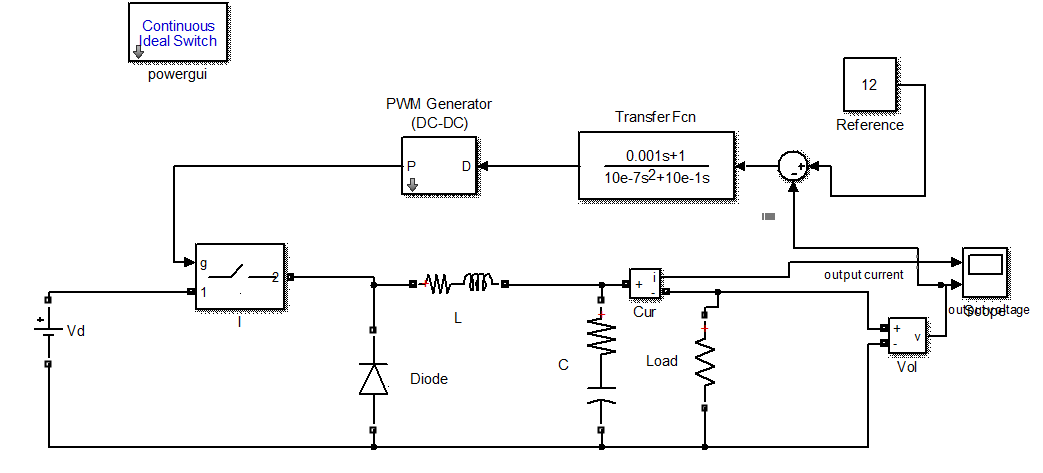


Figure 2.6: Bode plot of the designed Type-2 compensator

From this point on, simulations are conducted on SIMULINK. As SIMULINK does not have opamp model, compensator is implemented as transfer function block and the resultant SIMULINK model can be seen in Figure 2.7.  Figure 2.7: SIMULINK blocks of the buck converter with compensator

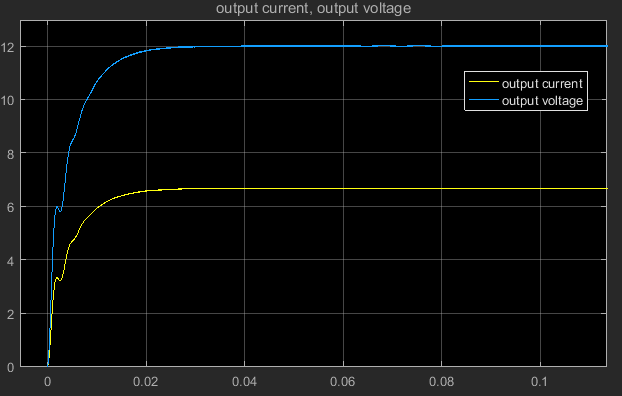


Figure 2.8: Transient response of the converter with compensator

Transient response of the converter with compensator can be seen in Figure 2.8. As can be seen in this figure, converter voltage rises the desired value at 0.02 s with no overshoot and oscillation and zero steady state error. Therefore transient response of this converter- compensator pair can be considered as stable and enough for many applications.

**d)**

In order to verify the performance of the controller, load increased half to full suddenly in this step. As seen from Figure 2.9 SIMULINK blocks are constructed in such way that at t=3 load side switch is closed and output load resistor decreased to 1.8Ω to 3.6Ω. The resultant output voltage and current waveforms can be seen in Figure 2.10.

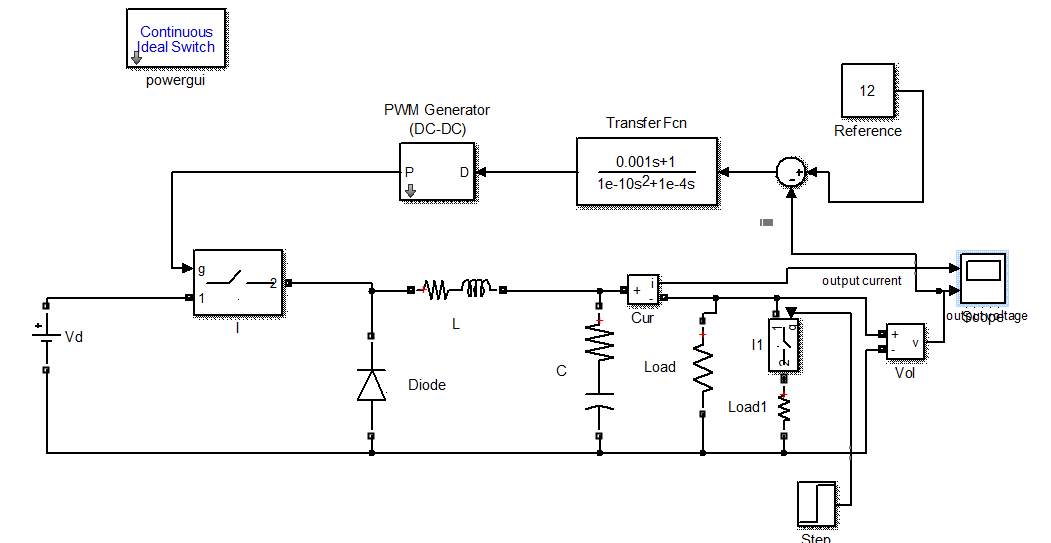
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Figure 2.9: SIMULINK blocks of implementing step change to full load from half load

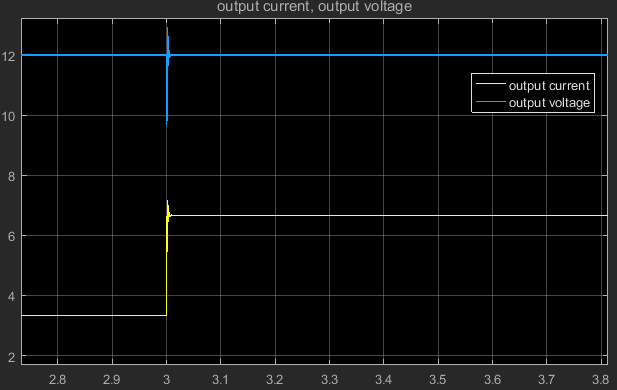
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Figure 2.10: The change in the output waveforms when step change to full load from half load

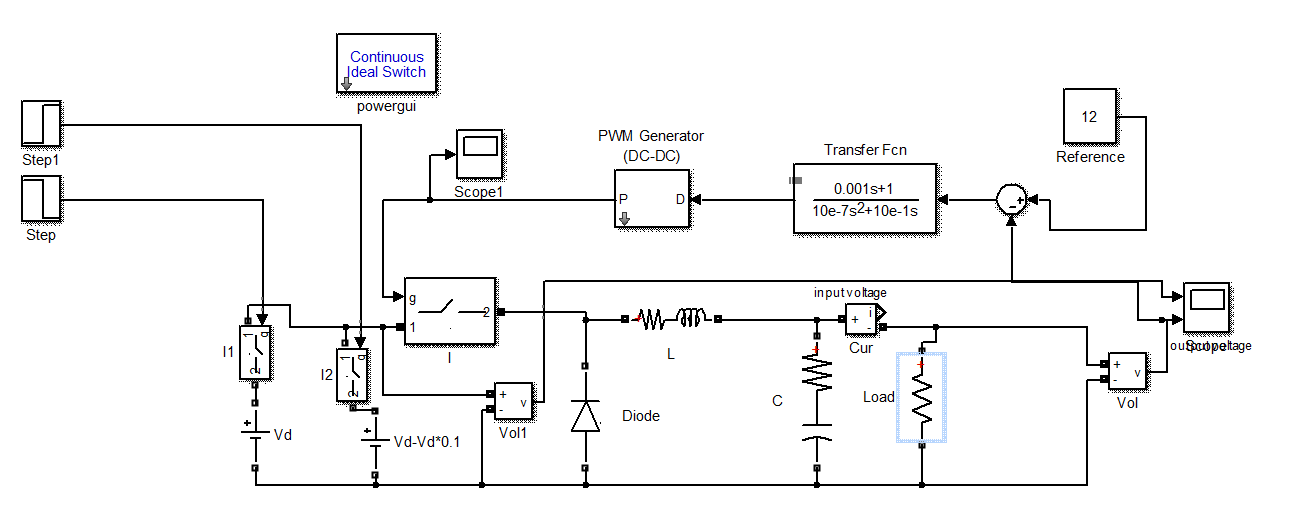
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Figure 2.11: SIMULINK blocks of implementing step change to decreased input voltage

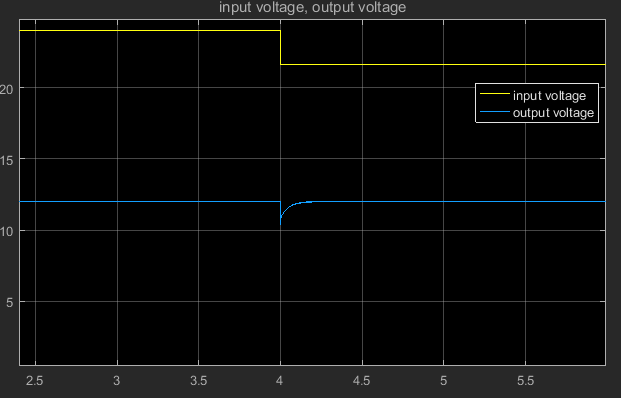


Figure 2.12: The change in the waveforms when step change to decreased input voltage

**e)**